

MTM86627A

Silicon P-channel MOS FET (FET)
Silicon epitaxial planar type (SBD)

For DC-DC converter circuits
For switching circuits

Overview

MTM86627A is the composite MOS FET (P-channel MOS FET and schottky barrier diode) that is highly suitable for DC-DC converter and other switching circuits.

Features

- Built-in schottky barrier diode: $V_R = 20\text{ V}$, $I_{F(AV)} = 800\text{ mA}$
- Low drain-source ON resistance:
 $R_{DS(on)} = 80\text{ m}\Omega$ (typ.) ($I_D = -1.0\text{ A}$, $V_{GS} = -4.0\text{ V}$)
- Low short-circuit input capacitance (common source): $C_{iss} = 300\text{ pF}$
- Small surface mounting halogen-free package:
WSSMini6-F1 (1.6 mm × 1.6 mm × 0.5 mm)

Absolute Maximum Ratings $T_a = 25^\circ\text{C}$

	Parameter	Symbol	Rating	Unit
FET	Drain-source surrender voltage	V_{DSS}	-20	V
	Gate-source surrender voltage	V_{GSS}	± 10	V
	Drain current	I_D	-2.0	A
	Peak drain current	I_{DP}	-8.0	A
	Channel temperature	T_{ch}	150	$^\circ\text{C}$
	Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
SBD	Reverse voltage	V_R	20	V
	Forward current (Average)	$I_{F(AV)}$	800	mA
	Non-repetitive peak forward surge current *1	I_{FSM}	3	A
	Junction temperature	T_j	125	$^\circ\text{C}$
	Storage temperature	T_{stg}	-55 to +125	$^\circ\text{C}$
Overall	Total power dissipation *2	P_D	540	mW

Note) *1: 50 Hz sine wave 1 cycle (Non-repetitive peak current)
*2: Measuring on ceramic substrate at 40 mm × 38 mm × 0.2 mm
Absolute maximum rating without heat sink for P_D is 150 mW

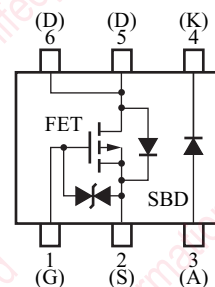
Package

- Code
WSSMini6-F1
- Pin Name

- | | |
|-----------|------------|
| 1: Gate | 4: Cathode |
| 2: Source | 5: Drain |
| 3: Anode | 6: Drain |

Marking Symbol: QK

Internal Connection



■ Electrical Characteristics $T_a = 25^\circ\text{C} \pm 3^\circ\text{C}$

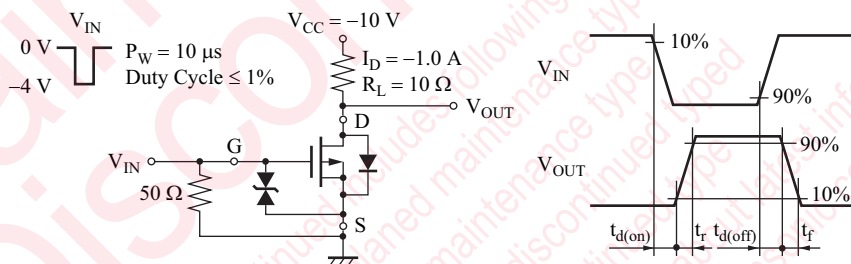
• FET

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	V_{DSS}	$I_D = -1.0 \text{ mA}, V_{GS} = 0$	-20			V
Drain-source cutoff current	I_{DSS}	$V_{DS} = -20 \text{ V}, V_{GS} = 0$			-1.0	μA
Gate-source cutoff current	I_{GSS}	$V_{GS} = \pm 8 \text{ V}, V_{DS} = 0$			± 10	μA
Gate threshold voltage	V_{TH}	$I_D = -1.0 \text{ mA}, V_{DS} = -10 \text{ V}$	-0.4	-0.75	-1.1	V
Drain-source ON resistance 1 *1	$R_{DS(on)1}$	$I_D = -1.0 \text{ A}, V_{GS} = -4.0 \text{ V}$		80	120	$\text{m}\Omega$
Drain-source ON resistance 2 *1	$R_{DS(on)2}$	$I_D = -1.0 \text{ A}, V_{GS} = -2.5 \text{ V}$		100	170	$\text{m}\Omega$
Drain-source ON resistance 3 *1	$R_{DS(on)3}$	$I_D = -0.5 \text{ A}, V_{GS} = -1.8 \text{ V}$		140	230	$\text{m}\Omega$
Forward transfer admittance *1	$ Y_{fs} $	$I_D = -1.0 \text{ A}, V_{DS} = -10 \text{ V}, f = 1 \text{ kHz}$	3.0			S
Short-circuit input capacitance (Common source)	C_{iss}			300		pF
Short-circuit output capacitance (Common source)	C_{oss}	$V_{DS} = -10 \text{ V}, V_{GS} = 0, f = 1 \text{ MHz}$		30		pF
Reverse transfer capacitance (Common source)	C_{rss}			35		pF
Turn-on delay time *2	$t_{d(on)}$	$V_{DD} = -10 \text{ V}, V_{GS} = 0 \text{ V to } -4 \text{ V},$ $I_D = -1.0 \text{ A}$		6		ns
Rise time *2	t_r			8		ns
Turn-off delay time *2	$t_{d(off)}$	$V_{DD} = -10 \text{ V}, V_{GS} = -4 \text{ V to } 0 \text{ V},$ $I_D = -1.0 \text{ A}$		57		ns
Fall time *2	t_f			55		ns

Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 measuring methods for transistors.

2. *1: Pulse measurement

*2: Measurement circuit

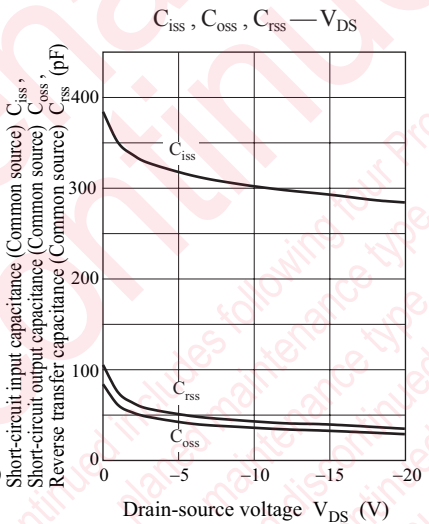
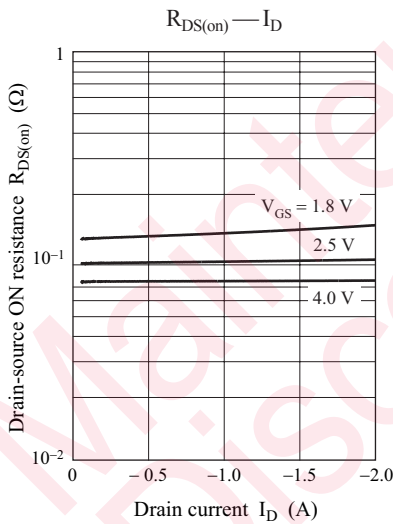
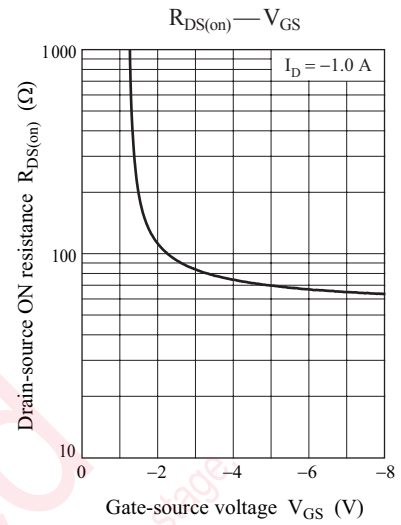
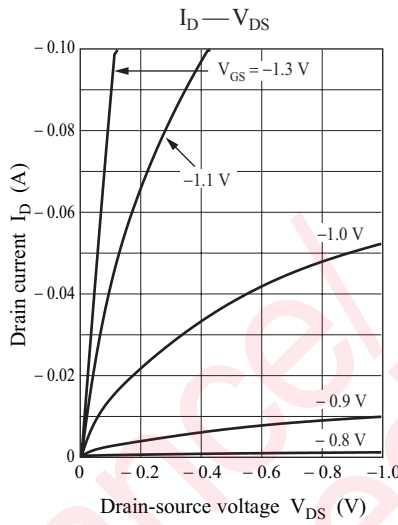
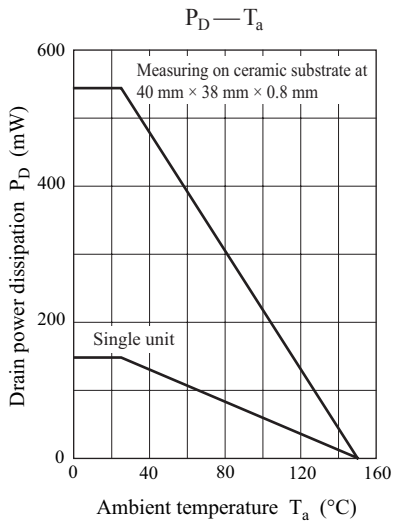


• SBD

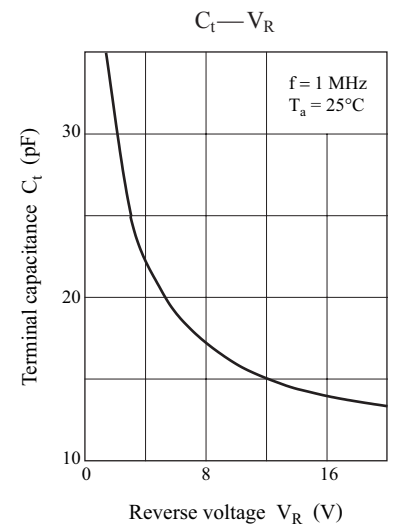
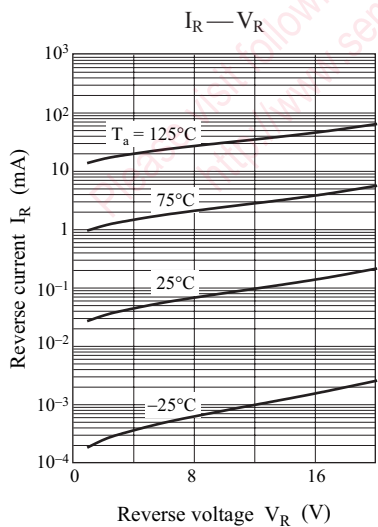
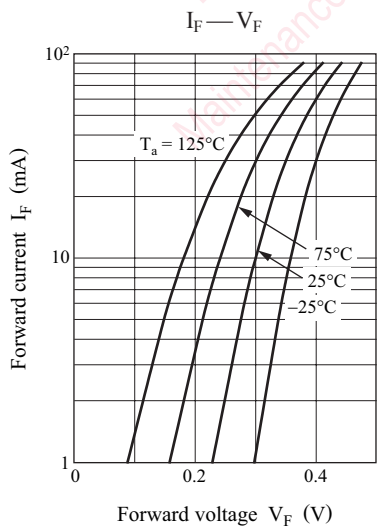
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Forward voltage	V_F	$I_F = 800 \text{ mA}$			0.47	V
Reverse current	I_R	$V_R = 20 \text{ V}$			80	μA

Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7031 measuring methods for diodes.

Characteristics charts of FET

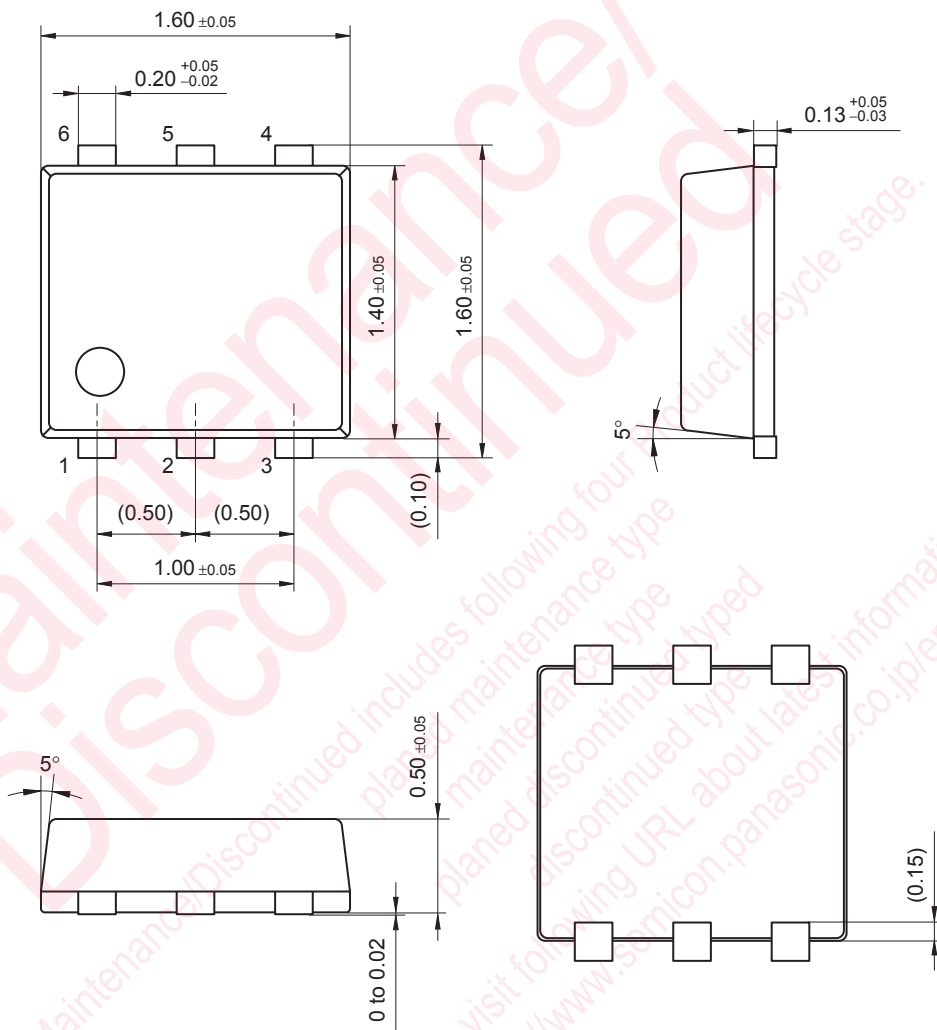


Characteristics charts of SBD



WSSMini6-F1

Unit: mm



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